Bench Test of First TRIP-t Prototypes

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Abstract A report of the bench tests of the first TRIP-t chips, with a short summary of how the chip should be operated.

Description of the TRIP-t

The TRIP-t chip, designed by Abderrezak Mekkaoui, is part of the front end of the D0 electronics for the VLPC based detectors. Its inputs are the analog pulses from the fibers after amplification by the VLPCs and digital timing inputs to control *e.g.* the time window over which the system should be sensitive to pulses. The outputs of the TRIP-t are (1) a digital signal to use for triggering; (2) an analog pulse (~1V) that is proportional to the amplitude of the input from the VLPC, called the A-pulse; (3) an analog pulse (~1V) that is proportional to the time between the firing of the discriminator and the closing of the time-gate, called the t-pulse.

The TRIP-t is a modification of the TRIP chip; see D0 notes 4009 and 4076. Documentation is at `smb://D0server6/projects/TriggerElectronics/CAE/Run_IIb_AF`. The the design requirements are in appendix 1

Figure 1 shows a simplified functional diagram of the TRIP-t. The front end, shown in simplified functional form in Figure 2, produces the three primary outputs of the chip. The A-pulse and t-pulse outputs are stored in 48 bucket deep analog pipelines which have a gain of 3, and the output of these is selected by the SKIPB signal, which is in effect the L1 ACCEPT signal. Outputs to form trigger signals are created by discriminators in the front end, and readout quickly through the digital multiplexer at a time determined by the DIGENU signal for channels 1-16 and the DIGENL signal for channels 17-32. To have both DIGENU and DIGENL asserted simultaneously is not allowed during regular operation and under these conditions the cell number accessed by the pipeline is sent to the discriminator output, starting at the high bit and going down, provided the pipeling depth is not zero. The operation of the front end is controlled by a set of DACs that determine parameters such as the drive currents for opamps. Although it is not shown in Figure 1, the Program Interface also provides some parameters to the pipeline and the final output drivers of the A- and t-pulses.

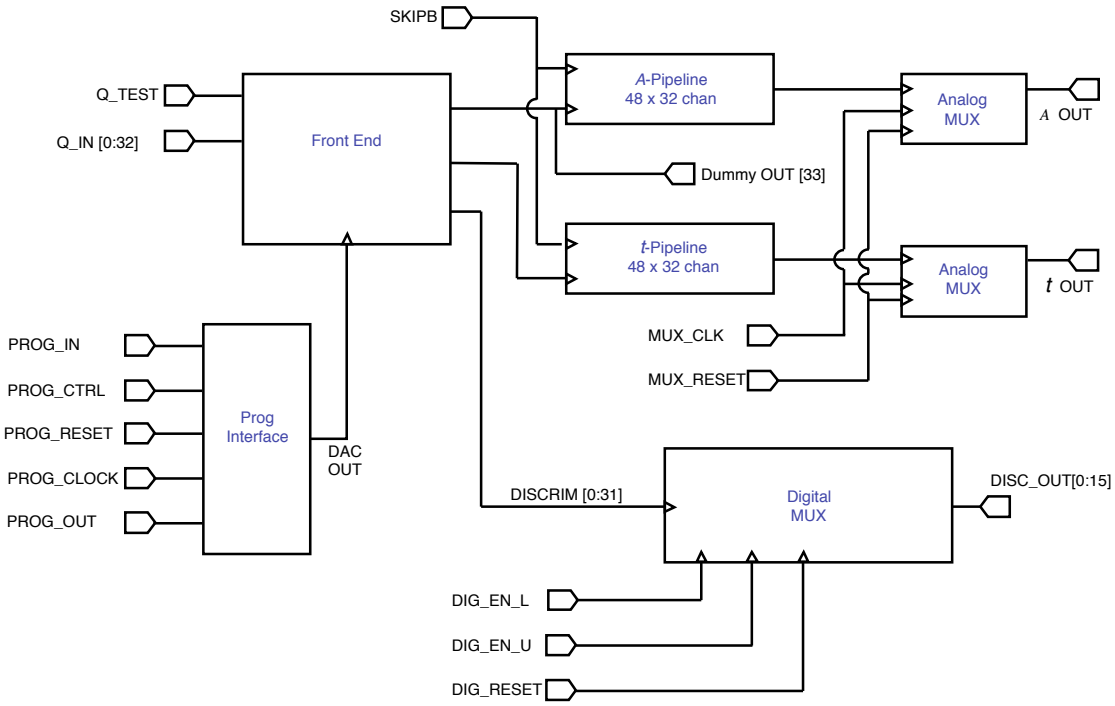

Figure 1. Simplified functional diagram of the TRIP-t

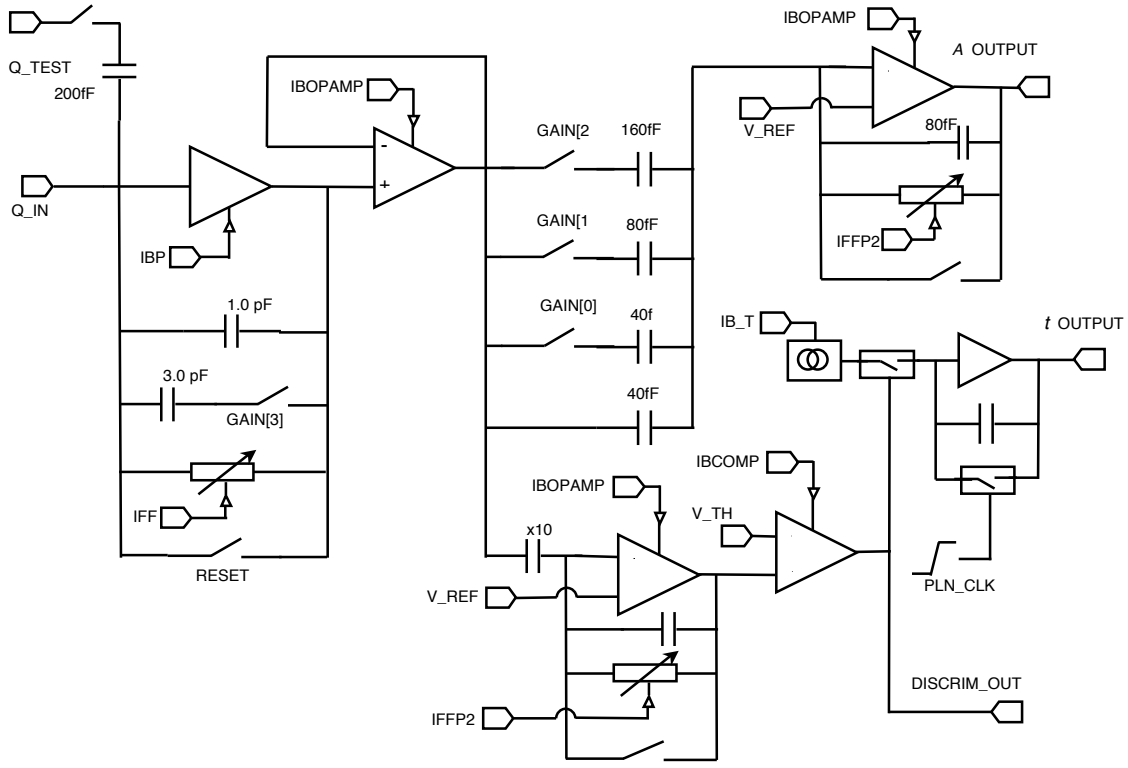

Figure 2. Simplified functional diagram of the TRIP-t front end.

Operation of the TRIP-t

The programing of the DACs for the TRIP-t is basically the same as it was for the TRIP chip, and is described in D0 note 4009. However, the meanings of the registers given in that document have changed. The new definitions and the values used here are given in Table 1. The values used here should be close to those used in the final installation, except for registers 6 and 11.

Register	Name	Default value	Comment
1	IBP	130	Preamp drive current
2	IBBNFoll	120	Preamp feedback control
3	IFF	40	Preamp feedback control
4	IBPIFF1REF	160	Preamp reset strength
5	IBOPAMP	255	Opamp drive current
6	IB_T	80	Time circuit current source
7	IFFP2	42	Opamp feedback control
8	IBCOMP	10	Comparator drive current
9	V_REF	170	Ref voltage for opamps 2 & 3
10	V_TH	243	Ref voltage for comparator
11[5:0]	PIPEDELAY	6	Pipeline depth
11[9:6]	GAIN	0111	Gain; high bit is negative logic
12	IRWSEL	15	Drive currents for pipeline R/W
13	LUCKB	42	Do not use
14	INJECT	Varies	Which channels to test-pulse

Table 1. Register settings use here. In situ, IB_T will be near 60 to provide an 80nsec range for the *t*-pulse, and PIPEDELAY will be 31. As described under "Follow-up tests" a better value for R_3 = IFF is zero.

Correct operation also requires specification of the timing of the signals input to the chip. A spreadsheet showing all the signals is available at `smb://D0server6/projects/TriggerElectronics/CAE/Run_IIb_AFE/Trip-t\ Chip/TRIP-t\ from\ Leo/Review_Apr05/DG2020\ copy.xls`. Figure 3 shows a detail of the critical reset/gating signals. The value of RefRes, which controls the size of the quantum for the DAC-controlled currents supplies, was 690kΩ.

A related issue is the capacitances used to couple the VLPCs to the AFE boards. In AFEI, capacitances between 12 and 470 pF were inserted on different boards, resulting in (effectively) different gains by virtue of the typically 35pF stray capacitance to ground of the flex cable. With the TRIP-t, we will be able to use 470pf across the boards and not have to shunt any of the VLPC output to ground.

Power was supplied at 2.5V on the lines VDDD and VDDA; the former draws typically 3-mA and the latter draws typically 103mA, giving a total power consumption under 265mW. Differing values of R_6 = IB_T change the balance of power between VDDD and VDDA but not the total.

The preamplifier reset signal is actually three signals; PRE_RST itself, and two inverted signals, P2A_RSTB and P2B_RSTB. All have the same timing; the reset is on for 245ns and then off for 155ns, making a cycle time of 400ns, close to the 396ns beam crossing time. The switching noise of the preamplifier reset limits the number of channels that can be connected to each other through their test inputs to 5. The signals DIGENL, DIGENU, and DIG_RSTB are 20ns wide and their positioning inside the PRE_RST pulse is not critical. The PLN_CLK signal determines the gate for which the input is sensitive, unless PR1 was high at an earlier low to high transition of PLN_CLK. In the latter case, the pipeline is read out. In figure 3, the chip will be sensitive to pulses at the input between t = 9420ns and t=9520ns. PRE_RST must finish 50ns before the PLN_CLK is active, and there is a 5ns gap after the gate closes before the next PRE_RST begins.

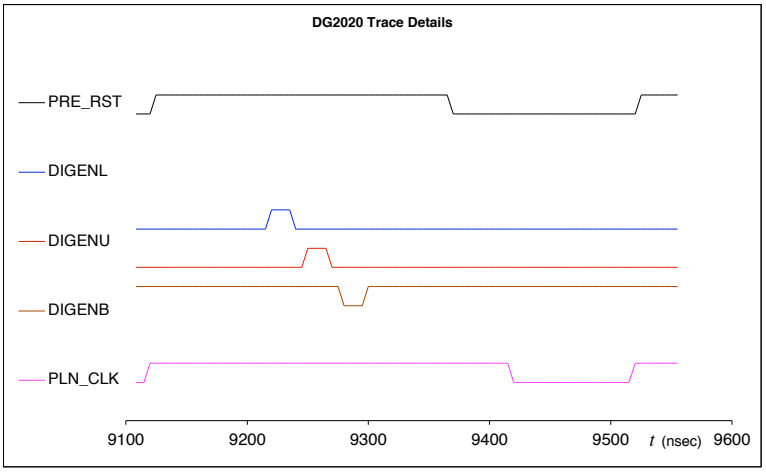

Figure 3. Reset and gating signal details

Discriminator test results

The setting of register R_{10} in Table 1 corresponds to a discriminator threshold of 8fC, assuming that the 200fF capacitor on the Q_TEST line of Figure 2 is indeed 200fF. Channel to channel variation of the capacitance within a given chip should be quite small – on the order of 5% – but the absolute scale of these capacitances is guaranteed to only the 30% level. Figure 4 shows the discriminator turn-on curves for 32 channels. The curves fit a Gaussian distribution well. Figure 5 shows the distributions of the fitted means and widths. Thresholds were measured with realistic (10pF) capacitances on the outputs.

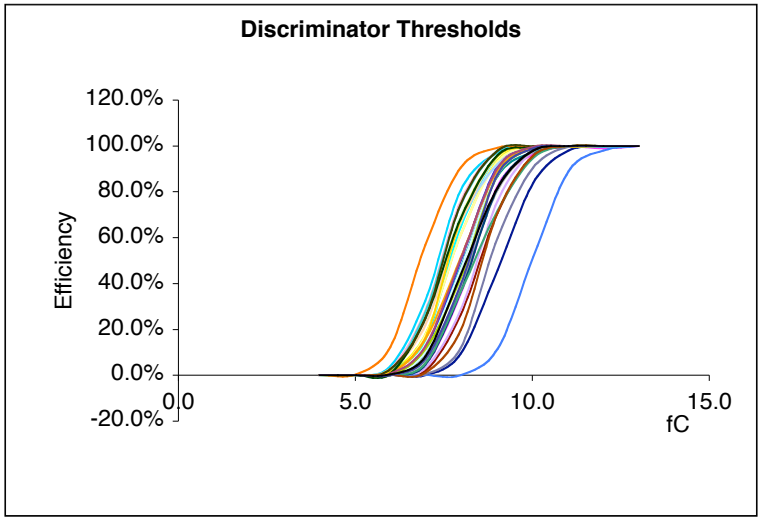

Figure 4. Discriminator threshold curves.

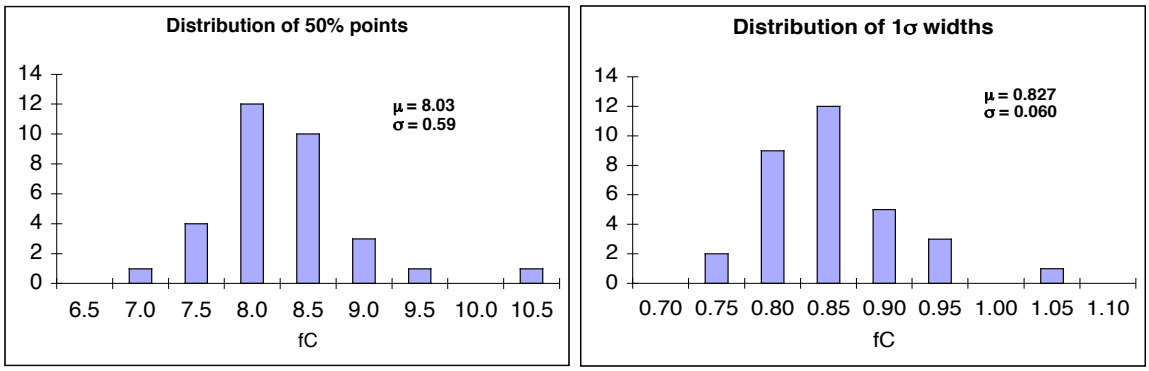

Figure 5. Distributions of fitted means and widths of the dicriminator turn-on curves for 32 channels.

A-pulse test results

There was a design problem with the *A*-pulse outputs, created by the final output drivers at the end of the pipeline. The problem seems easy to remedy.

First we show the distribution of *A*-pulse outputs as a function of time in the window, in Figure 6, for 5 channels. This result is essentially the same as for the TRIP; the rise time is essentially the width of the injected test pulse and the roll-off reflects the bandwidth of the preamp. Generally, *A*-pulse data shown here was taken at $t = 35ns$ on Figure 6.

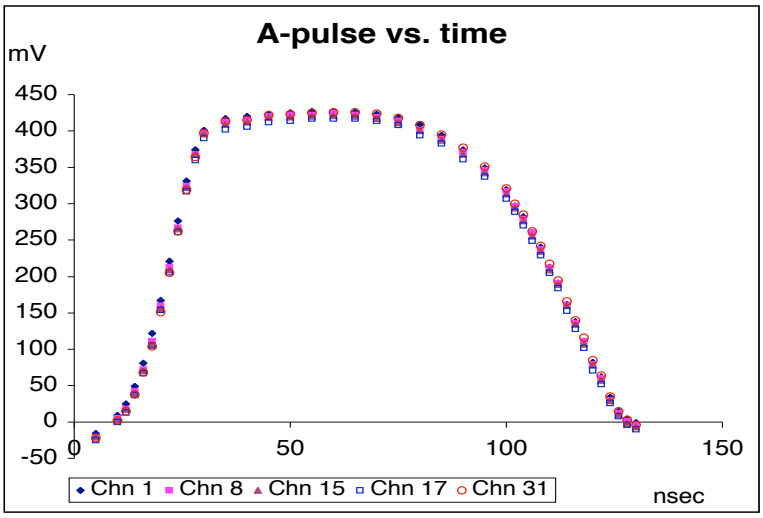

Figure 6. Pulse window for 100ns gate.

Figure 7 shows the A-pulse output as a function of injected charge for the highest gain setting, which is the gain planned for use in the fiber tracker. Note the

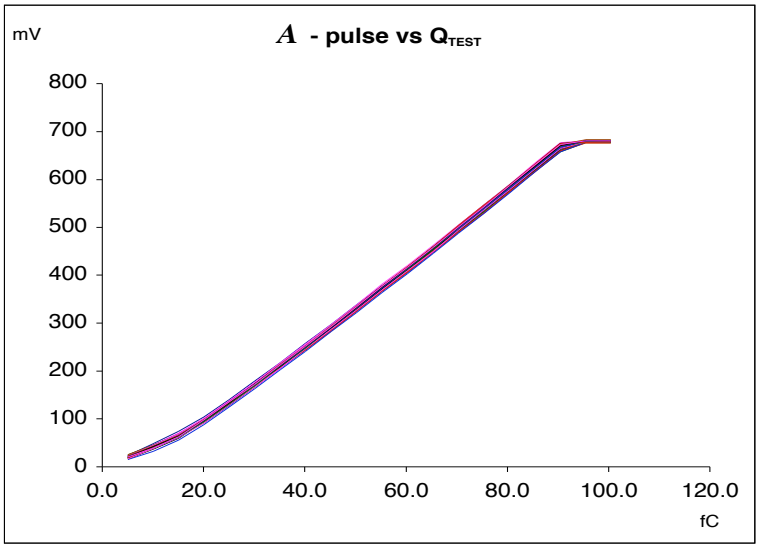

Figure 7. Nonlinearity in A-pulse outputs.

nonlinearity at low pulse amplitudes[1]. Figure 8 shows the differential gain, *i.e.*, the derivative of the curves in Figure 7. In the range below 40 fC, the differential gain drops off, finally going down to nearly half the correct value.

[1] Noise levels on the A-pulse and t-pulse outputs was Gaussian, with about 3mV RMS under most circumstances. There was no effort at distinguishing true noise in the TRIP-t from noise induced by the test setup.

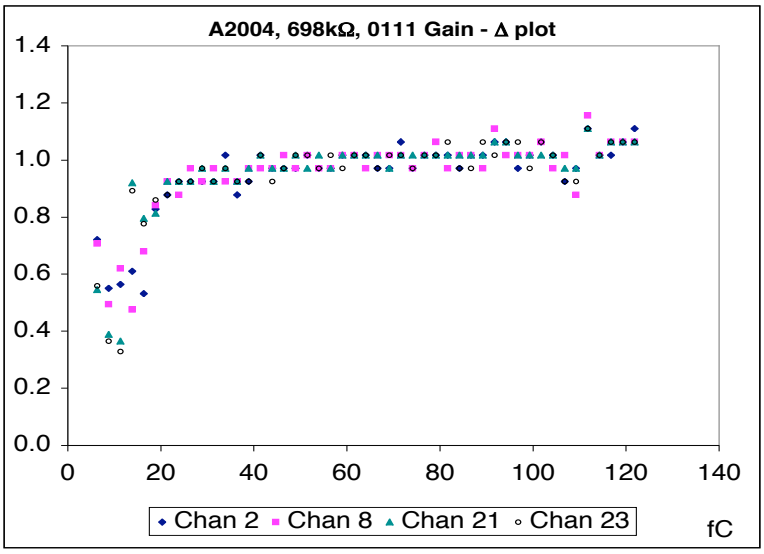

Figure 8. Nonlinearity in A-pulse differential gain.

The nonlinearity is well modeled in SPICE simulation. The left side of Figure 10 shows the simulated version of Figure 8. The curve OUTAP refers to the output of the analog pipeline; OUTAPBUF is the output of the final driver buffer that follows the pipeline. On the right side of Figure 10, the same curve is shown but with n channel FETs in the output buffer replaced p channel FETs, as shown in Figure 11.

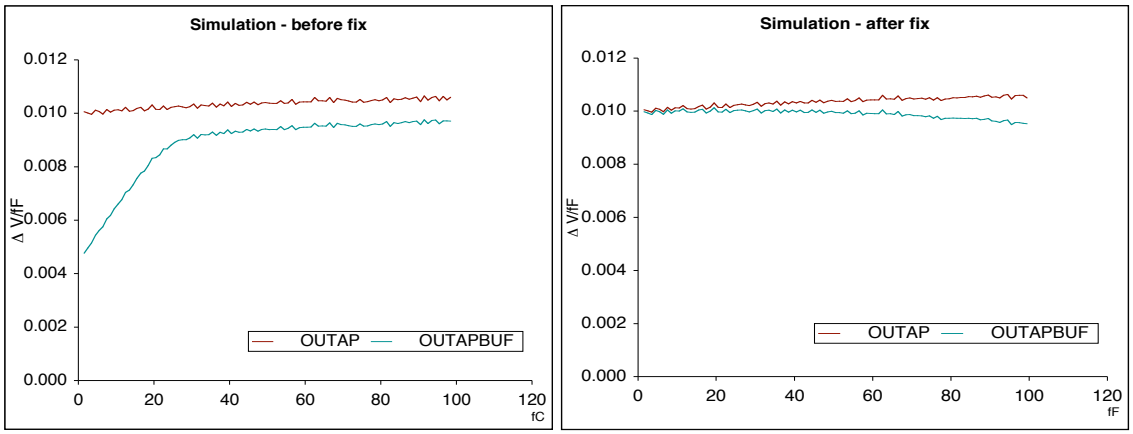

Figure 10. Differential gain in SPICE simulation of pipeline output buffer before and after FET revision. No capacitive load at the output has been allowed for.

The performance specification is accuracy equivalent to a7 bit ADC. Figure 12 shows the residual of a linear fit to the integal of the OUTAPBUF curve from the right side of Figure 9. The maximum residual occurs at full scale and is about

$5mV$; 7 bits precision on a 1V signal[2] is $7.8mV$. Simulations done later with ELDO yield a maximum residual of 1.0% of the full scale output, and with NANOSIM, about 0.7%.

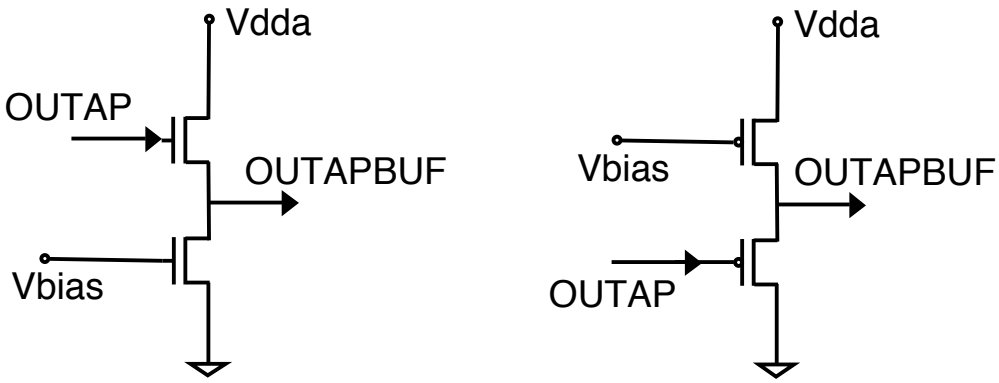

Figure 11. n channel to p channel FET substitution in final driver stage.

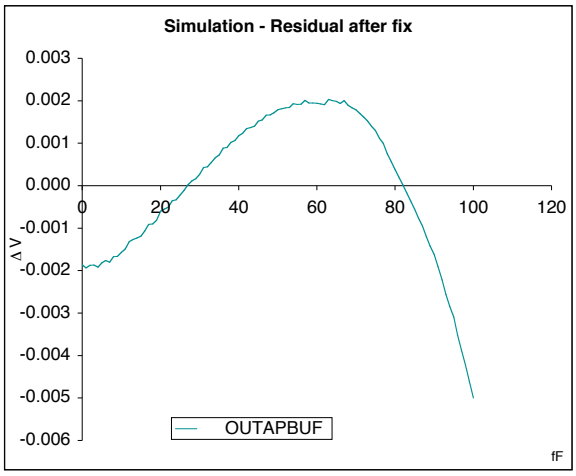

Figure 12. Residual nonlinearity in SPICE simulation after FET revision.

The gains of the 32 channels were determined by a fit of the measured responses in the region 45 to 85 fC. Figure 13 shows the distribution of gains. The intercepts themselves are not meaningful because of the non-linearity, but the scatter in the intercepts is aninteresting quantity as it says something about channel to channel uniformity, at least on the chip tested. The spread is $3.4mV$, not really different from the noise level itself. The spread in the points at the extreme left of Figure 7 is $2.7mV$.

[2] The running conditions in the SPICE simulation were slightly different than in the test bench runs.

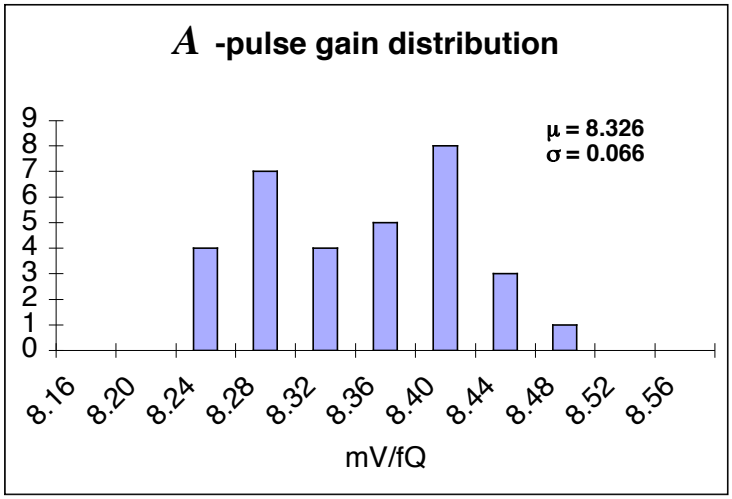

Figure 13. Distribution of measured gains.

t-pulse test results

The *t*-pulse output is created by switching the flow of current onto a capacitor at the time when the discriminator fires, and switching the flow off at the close of the gate (*i.e.*, at the low to high transition of PLN_CLK). The output, taken from this capacitor's charge, consequently becomes lower for later input pulses. Figure 14 shows the *t*-pulse output as a function of injection time for 45*fC* pulses. Some of the curvature visible at lower output values is undoubtably due to the output buffer issue, and before the correct selection of *t*-pulse gain can be done, the linearity of the output driver must be corrected.

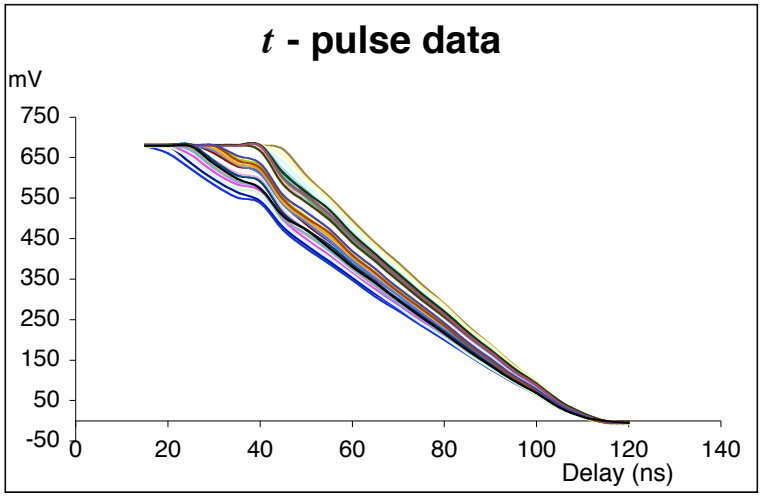

Figure 14. Measured *t*-pulse amplitudes as a function of injection time.

Gain variation is relatively larger in the t-pulse data than in the A-pulse data; selection of a final operation parameter for R_6 will also require adjustment to the channel of highest t-pulse gain. Figure 15 shows the distribution of gains after fitting the t-pulse curves to lines in the regions between 50 and 110ns

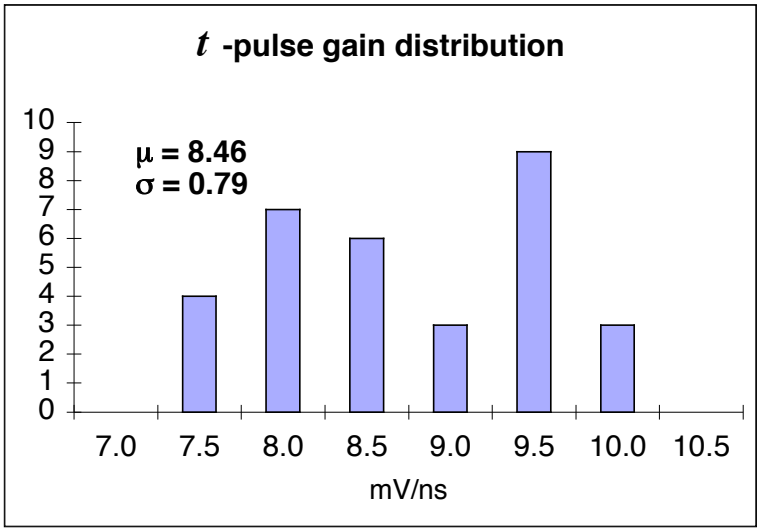

Figure 15. Distribution of gains of t-pulse outputs with 45fC input pulses.

The residuals of the t-pulse curves after fitting are shown in Figure 16. The RMS of the residual in this range is 8.3mV, corresponding to about 1ns.

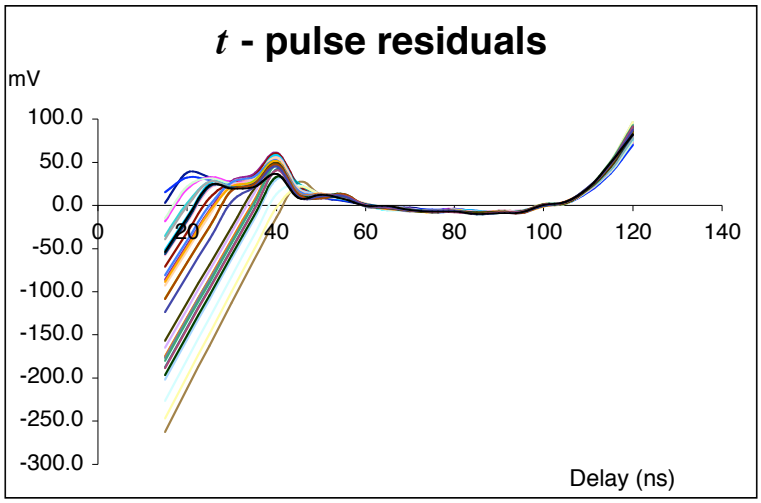

Figure 16. Residuals of t-pulse measurements after linear fit.

A minimum amplitude of pulse is necessary to get reliable t-pulse data. As shown in Figure 17, somewhere around a 30 to 40fC injected pulse is needed to keep the amplitude of the t-pulse independent of the amount of injected charge. Over that level, $\partial t/\partial A$ is about 0.55%, corresponding to shifts in the t-pulse corresponding to less than 1ns. Relative to pulse amplitude, $\partial t/\partial Q$ is about 49 $\mu V/fC$; the time shift appears to flatten out when the input pulse saturates the amplifier. Below that level, not only does the central value of the reported pulse time drift, there is a larger scatter in the amplitude of the t-pulses. Figure 18 is a plot of the dispersion in the t-pulse for small injected charges. It is derived by

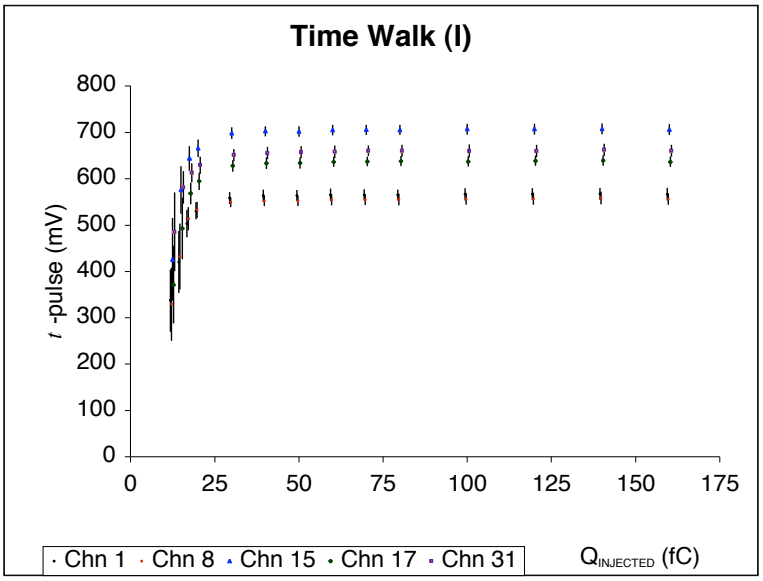

Figure 17. Variation in t-pulse measurements with changing injected pulse amplitudes.

taking the peak-to-peak spread of traces stored on an oscilloscope and dividing by three. This peak-to-peak reading technique was benchmarked against a set

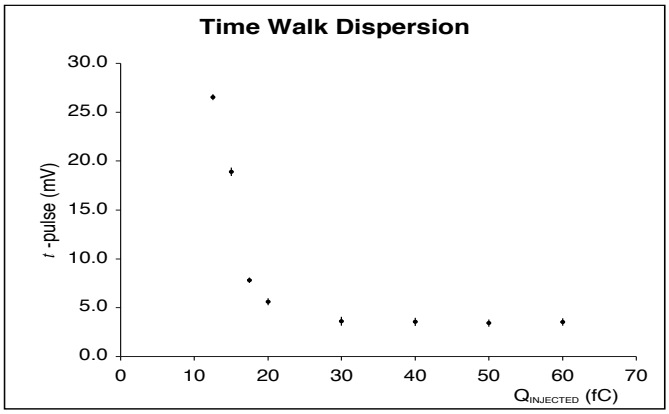

Figure 18. Approximate 1σ spread in t-pulse amplitudes as function of injected test pulse charge.

of 100 independent traces and found to actually return a 3σ spread of a Gaussian noise distribution to the ~10% level. The dispersion in the region plotted in Figure 18 is approximately 1290 exp(-Q_{INJ} /π), but extrapolation to lower charge levels is plainly unwise.

Follow-up tests

The data shown above are all from one single sample chip; another chip was operated under somewhat different conditions in the same period of time and nothing alarming was found, although a systematic study as shown above was not performed. Review of the data given above led us to ask some follow-up questions that were answered on a third chip. Not all of the test conditions here were theexactly same as in the previous tests, but changes have been noted and are of limited significance.

1) <u>What is the temperature sensitivity?</u>

The A-pulse, t-pulse, and discriminator thresholds of a few channels were examined as the chip was heated via hot-air gun held a meter or two away. The temperatures were forced to vary 5 to 10 degrees C and the temperature of the test board's ground plane was measured. The temperature variations *in situ* are normally within 2 degrees C, and fluctuate by as much as 5 C after the airflow has been disconnected to service the existing boards. The time required to reach thermal equilibrium has in the past been an uptime issue.

The A-pulse of channels 1, 15 and 21 of the chip showed no variations at the ~1mV level over temperature excursions of, in one case, 10 degrees. The t-pulse output of channel 15 shifted 3.3mV/C, and the pulses of channels 21 and 24, while not precisely measured, were seen to shift at a similar rate. At these settings, 3.3mV is about 0.4ns.

The discriminator threshold of channels 24 and 31 were measured at 25 and 33C. For channel 24, the threshold given by the fit went from 13.2fC to 13.0fC; for channel 31, from 12.9fC to 12.7fC. The widths remained unchanged at 1.2fC in channel 24; for channel 31, 1.1fC went to 1.3fC, but this is probably the limit of our ability to measure the widths as much as a real effect.

2) <u>Are IFF (R_3) and IFFP2 (R_7) set optimally?</u>

Examination of Figure 6 for gate widths of 150ns lead us to ask if we might not obtain a more uniform flat-top to the A-pulse if we lowered the values of ,the feedback resistors for the 1st and 2nd stage of the front end. The value of R_7 did not have any appreciable effect on the flatness of the flat-top, but IFF (R_3) did. The quantity ΔV, defined as the change in A-pulse value between the start of the flat-top (around 35ns in Figure 6) and then end thereof for at 150ns gate was measured as a function of the value of $R_3$with the result that, at least for the range R_3 = 0 to R_3 = 42, $\Delta V(mV) \approx 21.3 + 0.754\ R_3$. The original intent of the design was to allow for a continuous mode operation which is no longer needed;

we operated with $R_3 = 0$ henceforth. It should be possible, and is desirable, to change the implementation of R_3 to permit even lower values of the current IFF for the setting $R_3 = 0$.

3) The time walk curves show *t*-pulse data as possible dependent upon the size of the *A*-pulse; but the upward slope in the flattop section of Figure 6 shows a possible inverse dependence. What gives?

Both the *t*- and *A*-pulse have dependencies on (at least) the time of charge injection, t_{INJ}, the amount of injected charge Q_{INJ} as well as the gain setting in R_{11} and the setting of the current mirror R_6 that determines the gain of the *t*-pulse. The time walk data show that the *partial* derivatives are

$$\partial A / \partial Q_{INJ} = 49 \frac{\mu V}{fC} \quad \text{and} \quad 0.56\% \, \partial A / \partial Q_{INJ} = \partial t / \partial Q_{INJ} .$$

Although we expected to have to make some offline correction to the *t*-pulse, these values are low enough that we ought to not have to do that. The slope to the flattop of Figure 6 says that

$$\partial A / \partial t_{INJ} = 0.71 \frac{mV}{ns}, \text{ which corresponds to } \partial A / \partial t_{INJ} = -8.6\% \, \partial t / \partial t_{INJ}$$

as the amplitude of the *t*-pulse decreases with t_{INJ}. The derivatives $\partial A / \partial t_{INJ}$ and $\partial A / \partial Q_{INJ}$ are fundamentally different entities. The adjustment of IFF for question 3 lead to (for the second chip, measured on a single channel) of

$$\partial A / \partial t_{INJ} = 0.40 \frac{mV}{ns} .$$

The variation of the *A*-pulse upon the value of IB_T was investigated on channel 11 with a 150*ns* wide gate. Table 2 shows the results.

IB_T	*A*-pulse (*t* = 10*ns*)		*A*-pulse (*t* = 60*ns*)	
	DISC on	**DISC off**	**DISC on**	**DISC off**
0	378 *mV*	379 *mV*	377 *mV*	372 *mV*
20	368	378	373	372
40	358	378	366	371
60	347	378	361	372
80	336	378	354	373
100	324	377	348	371

At both ends of the flattop, $\partial A / \partial IB\_T \cong -4.5\% \left(\partial t / \partial IB\_T \right)$. It is curious that at low values of IB_T, the flattop goes to zero slope, and that with the discriminators off, $\partial A / \partial t_{INJ}$ actually goes negative. There is no real understanding of this other than to conclude that we are not dealing with something simple like capacitive coupling on lead-out lines.

In terms of what is is needed for the application, the observed $\partial A/\partial Q_{INJ}$ of $49\mu V/fC$ corresponds to a shift of $\sim 5mV$ for a saturating pulse, which is just barely visible above the noise level. Values of $\partial A/\partial t_{INJ}$ on the order of $0.4mV/ns$ for a $100ns$ spread in pulse arrival times corresponds to a $40mV$ variations in the A-pulse data. This is large, but: (1) in the next iteration of the chip design, the zero-point setting of IFFP2 is changed, so that this effect can be reduced further; (2) for charge division applications, both pulses entering into the division calculation arrive at similar times, not counting hit pairs that are spread across supersector boundaries, where they might be as much as $10ns$ apart; (3) in the worst scenario, we can consider offline correction of A-pulse data based on t-pulse data, akin to what was originally planned for t-pulse data.

4) Are the thresholds sensitive to the number of channels fired?

The threshold curve for channel 21 was measured with test pulses on for channels 1, 15, 24 and 31, and then re-measured with these channels off. (the test injection circuitry is limited to reliably handle 5 channels per chip). With the other channels on, the threshold was at $13.5fC$, with a width of $1.1fC$; with the other channels off, the threshold was at $13.6fC$, with a width of $1.0fC$. Although the chip is not expected to work correctly under such circumstances, we also tried looking at channel 16 with all 32 channels firing. The DISC output for the DIGENU channels sometimes came up late, (this could be remedied by moving DIGENL a bit earlier) but the fraction of the time that it came up eventually was consistent with a threshold shift of a few tenths of a fC.

5) Are the thresholds sensitive to the time of the arriving pulse?

The threshold curve for channels 8, 15, 24 and 31 were measured with test pulses of $60fC$ amplitude with $R_3 = 0$ and a $150ns$ long PLN_CLK. Figure 19 shows the variation of the central part of the turn-on curves as a function of pulse

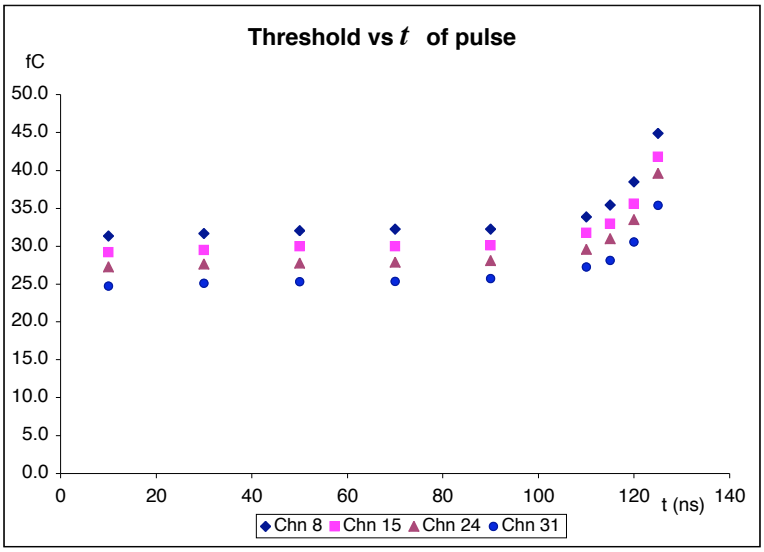

Figure 19. Discriminator firing threshold as a function of pulse arrival time.

arrival after the high-to-low transition of PLN_CLK. The measurent repeatability here is on the order of 1/4fC. The slew is less than 1fC up to 90 or 100ns.

6) How does the threshold (in fC) change with DAC What are the saturation points of the discriminator?

Again studying channels 8, 15, 24 and 31 with R_3 = 0 and a 150ns long PLN_CLK, Figure 20 shows the 50% point of the discriminator turnon curve as a function of discriminator DAC setting for the high gain in the preamplifier, *i.e.*, with gain bits 0111. For DAC settings down to about 60 (decimal), the threshold

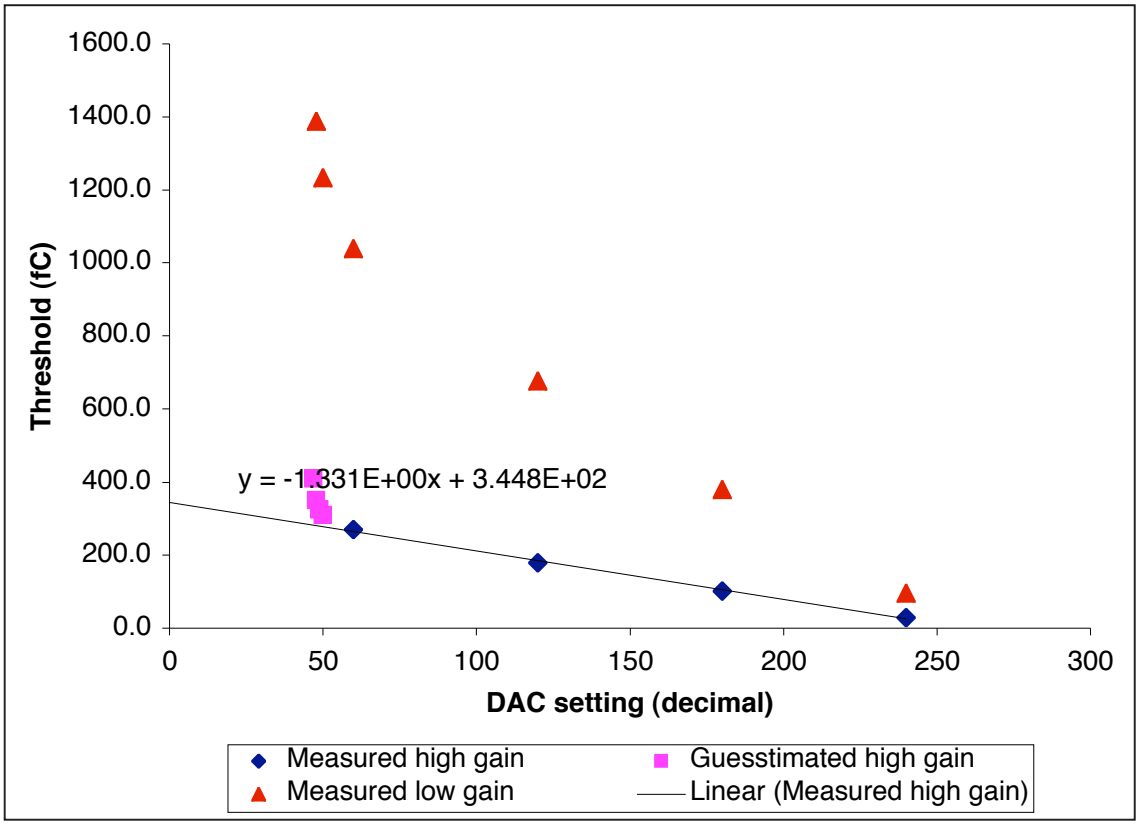

Figure 20. Discriminator turn-on points vs DAC setting.

moves linearly with DAC setting, changing about 1.33fC per DAC count. Below a DAC setting of 60 however, the preamp saturates and the saturation pulse amplitude is fed to the discriminator which will either fire or not depending on whether V_TH is above or below that amplitude. For the lower gain settings, only one channel was tested, because it is necessary to feed charge directly into the preamp rather than via the test pulse input. The result is also shown on Figure 20; again at DAC settings of 60 or so we see saturation. At the end of the linear region, we have thresholds of about 270fC at high gains and about 800fC at lower gains; the threshold moves about 4.8fC per DAC count at low gain.

7) How typical are the threshold data in Figures 4 and 5?

Fundamentally, this is a question about part tolerances and needs higher statistics than are available with this methodology. However, we did measure the thresholds of another chip under similar conditions to those in Figures 4 and 5. The second chip was either more sensitive to, or exposed to more, noise. The threshold 50% points averaged 0.51fC lower than in the earlier data (for the selected DAC setting) and the DC power supply was different for the second test. The higher noise level caused channels 1 and 3 to fire even at zero Q_{INJ} and 4 of the remaining 30 channels had abnormally wide turn-on curves, as shown in Figure 21.

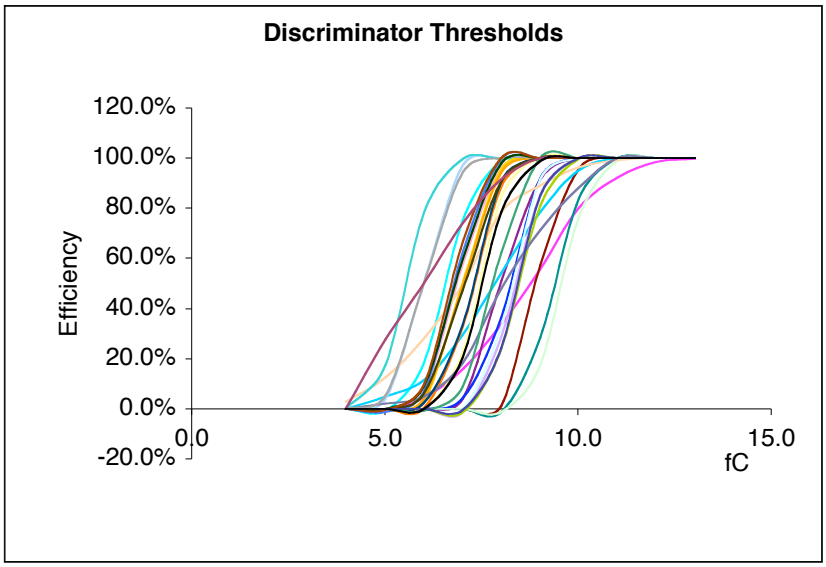

Figure 21. A second set of discriminator threshold curves.

Even including these 4 curves in the 2-chip average however, the spread in the 50% points is 0.82fC R.M.S; adding 0.51fC in quadrature leaves one well below the 4fC at 2.6σ spec. The average width of the turnon curve is 0.79fC, better than the 1fC spec. The lower 16 channels and the high 16 channels have the same thresholds to the statistical significance of the measurement, which is about 0.3fC.

8) How do the results vary with power supply voltage?

Looking at channel 17, we found that 0.1V changes in VDDD and VDDA changed the output of the A-pulse at or below the 1mV level, and the t-pulse output at the 3mV level. The discriminator output, as measured into a 50Ω line, shifted over a range of 0.24V; this corresponds to changes of the threshold of about 0.6fC.

Conclusion

A few TRIP-t prototypes have been bench tested at length. Operating parameters and input timing diagrams have been developed that are close to optimal for the existing design, and the performance has been characterized under these conditions. Two performance issues have ben found: the output driver stage that follows the analog pipeline is not as linear as needed, and the dependence of the A-pulse output upon the time of pulse arrival in the gate could be lower. These should both be fixed with the submitted chip design. Reliable t-pulse information, which will be of great use in the reconstruction, will be available for pulse that are about 4 to 5 photoelectrons over threshold[3]. Small sample bench tests doe not of course address (1) the statistical performance of large numbers of chips, (2) the reliability over extended periods of operation, and (3) performance in the actual operating environment.

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[3] A minimally ionizing particle at zero rapidity is produces a mean of about 8 photoelectrons in each fiber.

Appendix: Specs for TRIP-t

Revised: 9 May 2005 by PMR and LB w/ AP, DA, GG.

These specs are based on the observed performance of the TriP chip with the following changes:

- Bunch crossing rate = 396 ns. This gives the chip much more time in reset.
- Add a Time to Voltage converter:

This function should allow us to measure the time of the discriminator firing relative to the pipeline clock over a range of no less than 120ns with sufficient resolution such that effective LSB is to be 2ns or better after digitization.

The outputs of the T-to-V converter should be delayed by the same pipeline as the output of the integrator and should be muxed out on the same pins and the same way as the integrator analog outputs.

We expect the VLPCs and the fibers to degrade over time, so typical signals are lower than was expected for the TriP. Signal at high gain are 32fC and 6 pe (this corresponds to approximate VLPC gain of 32K). We also reduced the max test input charge- this cap is a parasitic on the input and should be kept small.

Channels per chip = 32 trigger + 32 analog + 32 timing

Window for charge collection (defined as the region where gain is flat within ±5%): from 50 to 150 ns, controllable. The typical window we expect to use is 100ns. All noise measurements will be made with this window.

Temperature range = 25 degC to 35 degC.

One adjustable gain setting per chip. All channels same gain.
(from G/2 to G*16 in steps of G/2)

HIGH GAIN

Input signals from Fiber Tracker or MIP layer of Preshower Detector.

- min: 1 photoelectron at 90 degrees incidence = 4 to 9 fC
- typ: 1 MIP at 90deg = 6 photoelectrons = 32 fC for Fiber Tracker
- 1 MIP = 65 fC for MIP layer of Preshower Detector
- max before saturation = 90 fC

Specifications at high gain (all numbers are input referred):

<u>Discriminators:</u>

- Threshold settable from 5fC to 90fC or more in steps of ~1fC.
- Noise (1σ width of the turn on curve): 1fC
- Threshold spread (measured at 50% point of turn on curve): 3fC within a chip max to min
- Temperature coefficient for threshold < 1fC / deg C

Analog output:

- Dynamic range 0 to 90fC with linearity of 7 bits
- Noise within the above range 1fC
- Allowed channel to channel gain spread (within one chip): +-5%
- Allowed channel to channel pedestal spread (within on chip): 10 fC
- Able to reset 3000fC without affecting the next crossing.

Timing output:

- Dynamic range 0 to 120nS with linearity of 7 bits (defined by external clock)
- Noise within the above range 2nS maximum
- Allowed channel to channel gain spread (within one chip): +-10%
- Allowed channel to channel pedestal spread (within on chip): 10 nS

LOW GAIN

Input signal from shower layer of Preshower Detector (at low gain = high gain/32):

- One 40 GeV electron or gamma at 45 degrees = 25 MIP per strip
  = 450 photoelectrons = 1890 fC for gain of ~26k
- max before saturation = 3000 fC = 40 MIP per strip at 45 degrees

Specifications at low gain (all numbers are input referred):

Discriminators:

- Threshold settable from 20fC to 200fC or more. This is a best-effort number; we anticipate that the CPS will want to set thresholds in the range 140-190fC.
- Noise (determined by fitting the turn on curve): 4fC
- Threshold spread: 12fC within a chip
- Temperature coefficient for threshold < 4fC / deg C

Analog output:

- Dynamic range 0 to 2850fC with linearity of 7 bits
- Noise within the above range 32fC
- Allowed channel to channel gain spread (within one chip): ±5%
- Allowed channel to channel pedestal spread (within on chip): 100 fC
- Able to reset 30000fC without affecting the next crossing.

Timing output:

- Dynamic range 0 to 120nS with linearity of 7 bits (defined by external clock)
- Noise within the above range 2nS maximum
- Allowed channel to channel gain spread (within one chip): +-10%
- Allowed channel to channel pedestal spread (within on chip): 10 nS

Other specifications:

Inputs:

- Fast (<1ns rise time), negative charge pulses, with input capacitance ~35pF

Analog outputs:

- 32 channels with analog multiplexers, balanced
- readout occurs ONLY in readout mode (not during acquisition mode)
- readout rate = 7.6 MHz or better.
- external load approx 10 pF

Digital outputs:

- 32 channels with 2:1 digital multiplexing for 16 unbalanced outputs.
- output in acquisition mode and only during integrator reset
- standard: LVCMOS2, 2.5V
- external load approx 10 pF

Test input:

- negative charge from 0 to 200 fC

- pulse time and width determined by CAL-INJECT
- pattern settable

Pipeline depth:

- 48 buckets programmable from 0 to 47

Power supplies:

- Power consumption < 10 mW per channel.
- Power supply: +2.5V, digital separate from analog.

The chip will be packaged.

Clocks provided to chip- no internal clock generation required.